REMARKS

The Examiner's Official Action dated February 4, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One Month Extension of Time* which extends the shortened statutory period for response to June 4, 2002. Accordingly, Applicants respectfully submit that this response is timely filed.

Claims 1-52 are pending in the present application, of which claims 1, 8, 15, 23, 31, 36, 42 and 48 are independent. Claims 1, 8, 15, 23, 31, 36, 42 and 48 have been amended herewith. For the reasons set forth in detail below, this application is believed to be in condition for allowance.

The Official Action has objected to the title for not being descriptive. In response, the Applicants have amended the title as follows: SEMICONDUCTOR DEVICE COMPRISING FIRST INSULATING FILM, SECOND INSULATING FILM COMPRISING ORGANIC RESIN ON THE FIRST INSULATING FILM, AND PIXEL ELECTRODE OVER THE SECOND INSULATING FILM. It is respectfully submitted that the new title is descriptive and favorable reconsideration is requested.

Independent claims 1, 8, 15, 23, 31, 36, 42 and 48 have been amended so as to include a feature of a first insulating film covering at least the gate electrode and the semiconductor layer except for contact holes opened therein. The claimed feature is directed to a TFT structure as shown in Fig. 2F and as supported in page 22 of the specification.

Paragraph 2 of the Official Action rejects claims 1, 2, 4, 6-9, 11, 13-16, 18, 20-24, 26, 28-30, 48, 49 and 51 as anticipated by U.S. Patent No. 5,424,244 to Zhang et al. The Applicants respectfully traverse the rejection and submit that Zhang does not teach or suggest all the elements of the independent claims, either explicitly or inherently.

The Official Action contends that Zhang teaches a first insulating film that is denoted by an anodically oxidized film (207) in col. 16, line 64 and in Fig. 11(B). Independent claims 1, 8, 15, 23 and 48 have been amended herewith so as to include a feature of a first insulating film covering at least the gate electrode and the semiconductor layer except for contact holes opened therein. This feature is also supported in Fig. 2F. It is respectfully submitted that Zhang fails to teach or suggest the first insulating film covering the semiconductor layer except for contact holes opened therein.

For the reasons stated above, the Examiner has not formed a proper anticipation rejection. Accordingly, reconsideration and withdrawal of the rejection of independent claims 1, 8, 15, 23 and 48 under 35 U.S.C. § 102(e) is in order and respectfully requested. Likewise, it is believed that dependent claims 2, 4, 6, 7, 9, 11, 13, 14, 16, 18, 20-22, 24, 26, 28-30, 49 and 51 are likewise allowable in that they depend from what is believed to be allowable base claims 1, 8, 15, 23 and 48.

Paragraph 3 of the Official Action rejects claims 1-4, 6-11, 13-18, 20-26, 28-30 and 48-51 as obvious based on the combination of U.S. Patent No. 5,153,142 to Hsieh, and U.S. Patent 5,273,910 to Tran. The Applicants respectfully traverse the Examiner's rejection because the Official Action has not made a *prima facie* case of obviousness.

The prior art, either alone or in combination, does not teach or suggest all the elements of the independent claims. The Official Action contends that it would have been obvious to form the layer (14) in the Hsieh device of a single crystal silicon layer instead of a polysilicon layer as taught by Tran. However, it should be noted that a single crystal silicon layer is not recited in any of the claims and thus this rejection is believed to be moot.

The Examiner further contends that it would have been obvious to coat the first insulating film (20) in Hseih's device with a polyimide layer (53) as taught by Tran in order to obtain a smooth planarization layer (col. 10, lines 8-32 of Tran). The Applicants respectfully disagree with the Examiner's contention for the following reason.

Independent claims 1, 8, 15, 23 and 48 have been amended to recite that a pixel electrode is formed over the second insulating film. On the other hand, Hsieh teaches the ITO pixel electrode (44) is formed on the first insulating film (20) as shown in FIG. 12. Tran fails to teach the pixel electrode. Hence, even if Hsieh and Tran are combined, the claimed feature of the present invention that the pixel electrode is formed over the second insulating film cannot be obtained.

For the reasons stated above, the Examiner has not set forth a *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejection of independent claims 1, 8, 15, 23 and 48 under 35 U.S.C. § 103(a) is in order and respectfully requested. Likewise, it is believed that dependent claims 2-4, 6, 7, 9-11, 13, 14, 16-18, 20-22, 24-26, 28-30 and 49-51 are likewise allowable in that they depend from what is believed to be allowable base claims 1, 8, 15, 23 and 48.

The Official Action next rejects claims 5, 12, 17, 19, 27, 31-47 and 52 as obvious based on the combination of Hsieh, Tran and U.S. Patent No. 5,027,185 Liauh. The Applicants respectfully assert that the Official Action has failed to establish a *prima facie* case of obviousness and requests reconsideration for the following reasons.

The prior art, either alone or in combination, does not teach or suggest all the elements of the independent claims. Similar to independent claims 1, 8, 15, 23 and 48, amended independent claims 31, 36 and 42 also recite that the pixel electrode is formed over the second insulating film. Liauh is relied upon because Liauh teaches conductive films, but Liauh also fails to teach the above claimed feature.

For the reasons stated above, the Official Action has not set forth a *prima facie* case of obviousness and reconsideration and withdrawal of the rejection of independent claims 31, 36 and 42 under 35 U.S.C. § 103(a) is in order and respectfully requested. Likewise, it is believed that dependent claims 5, 12, 17, 19, 27, 32-35, 37-41, 43-47 and 52 are likewise allowable in that they depend from what is believed to be allowable base claims 31, 36 and 42.

Having responded to all rejections set forth in the outstanding final Office Action, it is submitted that the claims are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

Please amend the title to read as follows:

[METHOD FOR MANUFACTUNG A SEMICONDUCTOR DEVICE]
--SEMICONDUCTOR DEVICE COMPRISING FIRST INSULATING FILM, SECOND INSULATING FILM COMPRISING ORGANIC RESIN ON THE FIRST INSULATING FILM, AND PIXEL ELECTRODE OVER THE SECOND INSULATING FILM--

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1, 8, 15, 23, 31, 36, 42 and 48 as follows.

1. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film [formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode] covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a pixel electrode formed over said second insulating film.

8. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film;

a first insulating film [formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode] covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a pixel electrode formed over said second insulating film.

15. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film [formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode] covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a transparent pixel electrode formed over said second insulating film.

23. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film;

a first insulating film [formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode] covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a transparent pixel electrode formed over said second insulating film.

31. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film [formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode] covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions.

36. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film [formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode] covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a transparent pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions.

42. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film [formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode] covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a transparent pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions, wherein said electrode comprises a same material as said conductive layer.

48. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first insulating film [formed over said insulating surface, said semiconductor layer, said gate insulating film and said gate electrode] covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed on said first insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions;

a pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions,

wherein a portion of said pixel electrode is located below said electrode.